
EXHIBIT B

A 1-kV 4H-SiC Power DMOSFET Optimized for Low ON-Resistance

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Abstract—In this paper we describe a low-voltage (~ 1 kV) short-channel 4H-SiC power DMOSFET with several structural modifications to reduce the specific ON-resistance. These include the following: 1) a heavily doped n-type current-spreading layer beneath the p-base; 2) a heavily-doped JFET region with narrow ($\sim 1 \mu\text{m}$) JFET width; 3) a “segmented” base contact layout; and 4) tighter alignment tolerances to reduce cell pitch. The design is optimized using computer simulations, and the resulting devices are fabricated and characterized. The fabricated device exhibits a specific ON-resistance of $6.95 \text{ m}\Omega \cdot \text{cm}^2$, which is one of the lowest yet reported ON-resistances for a power MOSFET in this voltage range.

I. INTRODUCTION

SINCE the introduction of the first SiC power DMOSFET in 1996, SiC power MOSFETs have made great progress [1]. Over this period, blocking voltages have increased from 760 V to over 10 kV [2]. However, there has been little progress in reducing the specific ON-resistance. In low-voltage (~ 1 kV) MOSFETs, the ON-resistance is limited by the resistance of the MOS channel, which is caused by the low mobility of inversion electrons at the SiO_2 /4H-SiC interface. Two developments have significantly reduced the channel resistance. First, the electrical quality of the interface has been improved dramatically, mainly due to the introduction of a postoxidation anneal in nitric oxide (NO) [3]. This has led to a fivefold increase in inversion layer electron mobility [4] and a corresponding reduction in channel resistance. Second, the introduction of a self-aligned process for the fabrication of short-channel DMOSFETs [5]–[7] has reduced the channel resistance to another factor of five. As a result, the specific ON-resistance of well-fabricated 4H-SiC power DMOSFETs is no longer limited solely by the channel resistance. In fact, simulations show that the channel resistance, JFET resistance, drift layer resistance, and source resistance play almost equal roles.

To make further progress, it is necessary to conduct a global optimization of the DMOSFET in a way that addresses all the limiting factors simultaneously. In this paper, we report a detailed simulation study to optimize the ON-state performance

of 1-kV SiC DMOSFETs, and experimental verification of the resulting optimized design.

II. DEVICE OPTIMIZATION

As stated above, the specific ON-resistance of the well-fabricated 1-kV 4H-SiC DMOSFETs is comprised of almost equal contributions from the MOS channel, the JFET region, the drift layer, and the source contact. The drift layer resistance is determined by the doping and thickness of the epilayer. Since these parameters also control the blocking voltage, it is not possible to change them in an arbitrary fashion. From 2-D simulations, it is found that electrons spread laterally in a trapezoidal fashion as they flow into the drift region from the narrow JFET region. The insertion of a thin heavily doped n+ current-spreading layer (CSL) beneath the p-type base region helps distribute the electron flow more uniformly, minimizing current crowding at the top of the drift region and reducing the drift layer resistance. Fig. 1 shows a cross section of the DMOSFET structure with the CSL. This CSL and the JFET region above are formed as n-type epitaxial layers having higher doping than the drift layer. The more heavily doped JFET region also helps reduce the ON-resistance. However, the addition of these two heavily doped regions causes an increase in the oxide field over the JFET region in the blocking state. MEDICI simulations show that if the JFET region width is reduced, more field lines terminate on the p-base regions, and the field in the oxide is reduced. This can only be carried so far, since beyond a certain point, the constriction of electron flow in the JFET region begins to increase the device ON-resistance. Thus, we seek a design that minimizes the ON-resistance without reducing the blocking voltage.

To optimize the device performance, we consider four design parameters: drift region doping (N_{epi}), CSL doping (N_{CSL}), JFET region doping (N_J), and JFET region width (W_J). A detailed analysis is performed using the Taguchi method [8] to determine the effects of each of these design parameters on three figures of merit: blocking voltage (V_B), specific ON-resistance $R_{\text{ON,SP}}$, and the parameter $V_B^2/R_{\text{ON,SP}}$. Blocking voltage is defined as the drain voltage at which the following conditions are true: 1) avalanche breakdown occurs, or 2) the field in the oxide reaches 4 MV/cm, whichever is less. In all the analyses reported here, we assume a channel length of $0.5 \mu\text{m}$, an inversion layer mobility of $20 \text{ cm}^2/\text{V} \cdot \text{s}$, and room temperature operation.

We find that JFET and epilayer dopings have the greatest effect on specific ON-resistance, while the JFET width has the greatest effect on the blocking voltage (by reducing the oxide

Manuscript received March 9, 2007; revised July 2, 2007. This work was supported by Defense Advanced Research Projects Agency under Grant N00014-05-5-0437, monitored by Office of Naval Research. The review of this paper was arranged by Editor M. A. Shibib.

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Digital Object Identifier 10.1109/TED.2007.904577

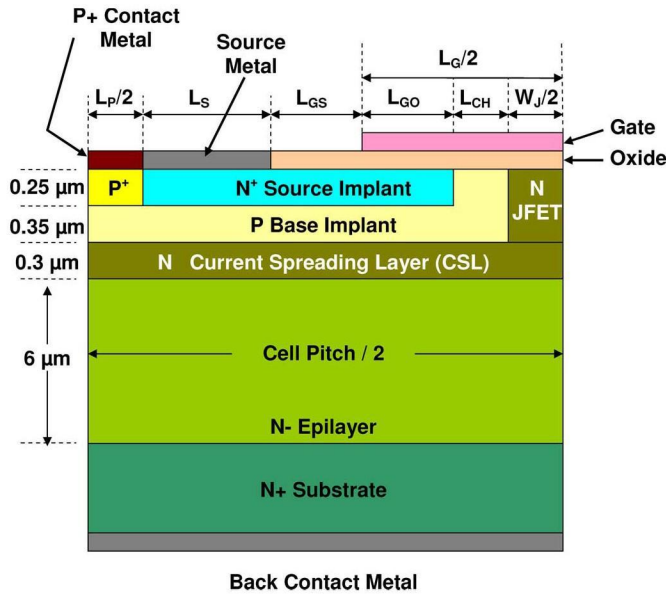
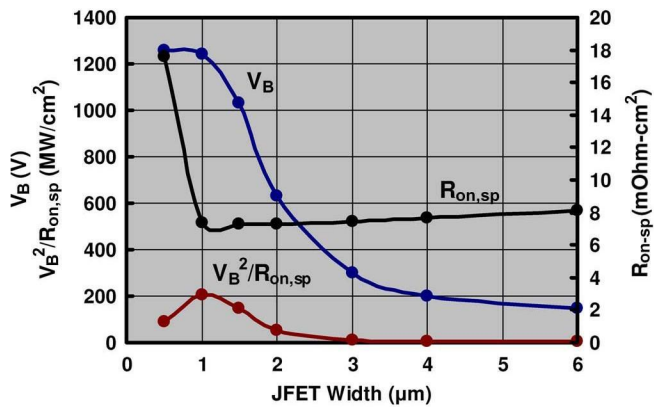
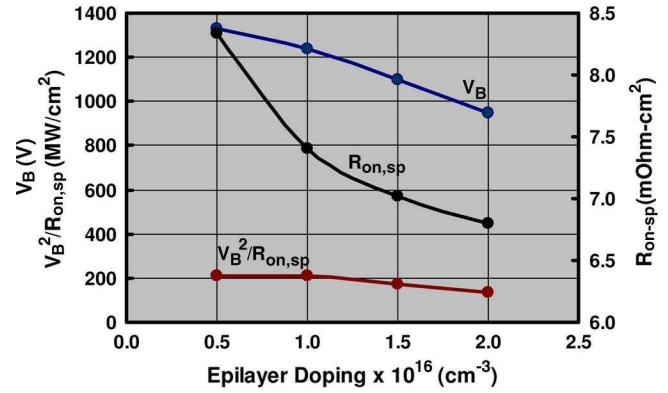
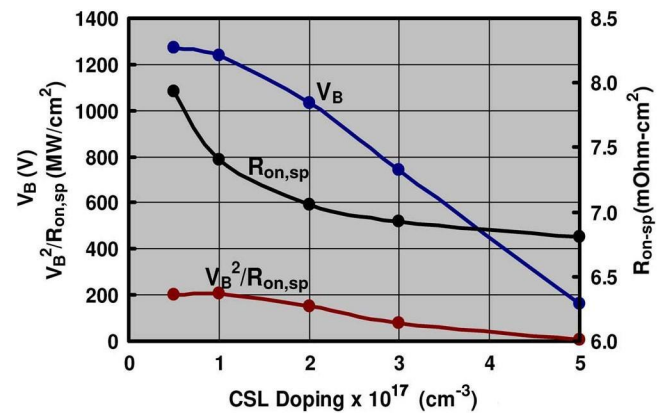
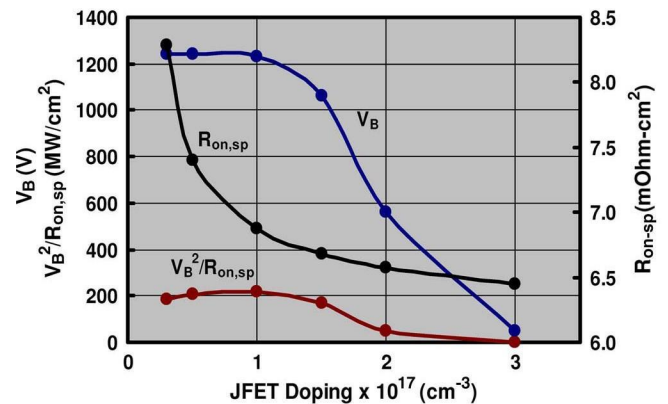


Fig. 1. Cross-sectional view of the DMOSFET cell.

Fig. 2. Variations of V_B , $R_{ON,SP}$, and $V_B^2/R_{ON,SP}$ with JFET width. In this comparison, $N_{epi} = 1E16 \text{ cm}^{-3}$, $N_{CSL} = 1E17 \text{ cm}^{-3}$, $N_J = 5E16 \text{ cm}^{-3}$; L_P , L_S , L_{GS} , and L_{GO} are $2 \mu\text{m}$ each, and $L_{CH} = 0.5 \mu\text{m}$.

field). The JFET width also has the strongest effect on the figure of merit $V_B^2/R_{ON,SP}$. Although it has a relatively small effect on either the blocking voltage or ON-resistance alone, the CSL doping has a strong effect on $V_B^2/R_{ON,SP}$. Figs. 2–5 show how the performance parameters V_B , $R_{ON,SP}$, and $V_B^2/R_{ON,SP}$ vary with each of the four design parameters W_J , N_{CSL} , N_J , and N_{epi} . In these figures, only one parameter is being varied at a time; therefore, these results do not represent a trajectory along the gradient vector in the 4-D parameter space of the Taguchi analysis.

The JFET width has a twofold effect on the specific ON-resistance. A smaller JFET width increases the resistance since it pinches off the current path, but it also reduces the cell area. As a result, the overall effect on the specific ON-resistance is nearly negligible, as shown in Fig. 2. JFET width has no effect on avalanche breakdown voltage, but a larger JFET width increases the gate oxide field sharply, reducing the oxide-limited blocking voltage. The optimum JFET width is approximately $1 \mu\text{m}$. At this design point, $V_B^2/R_{ON,SP}$ attains its maximum value, as shown in Fig. 2.

Fig. 3. Variations of V_B , $R_{ON,SP}$, and $V_B^2/R_{ON,SP}$ with epilayer doping. In this comparison, $W_J = 1 \mu\text{m}$, $N_{CSL} = 1E17 \text{ cm}^{-3}$, $N_J = 5E16 \text{ cm}^{-3}$; L_P , L_S , L_{GS} , and L_{GO} are $2 \mu\text{m}$ each, and $L_{CH} = 0.5 \mu\text{m}$.Fig. 4. Variations of V_B , $R_{ON,SP}$, and $V_B^2/R_{ON,SP}$ with CSL doping. In this comparison $W_J = 1 \mu\text{m}$, $N_{epi} = 1E16 \text{ cm}^{-3}$, $N_J = 5E16 \text{ cm}^{-3}$; L_P , L_S , L_{GS} , and L_{GO} are $2 \mu\text{m}$ each, and $L_{CH} = 0.5 \mu\text{m}$.Fig. 5. Variations of V_B , $R_{ON,SP}$, and $V_B^2/R_{ON,SP}$ with JFET doping. In this comparison, $W_J = 1 \mu\text{m}$, $N_{epi} = 1E16 \text{ cm}^{-3}$, $N_{CSL} = 1E17 \text{ cm}^{-3}$; L_P , L_S , L_{GS} , and L_{GO} are $2 \mu\text{m}$ each, and $L_{CH} = 0.5 \mu\text{m}$.

Increasing the epilayer doping reduces the drift layer resistance, but decreases the avalanche breakdown voltage. For a JFET width of $1 \mu\text{m}$, the blocking voltage is limited by avalanche breakdown for the entire range of epilayer dopings, as shown in Fig. 3. The optimum epilayer doping, in terms of $V_B^2/R_{ON,SP}$, is approximately $1 \times 10^{16} \text{ cm}^{-3}$.

Increasing the CSL doping helps distribute the current more uniformly into the drift region, thereby reducing the drift layer resistance, as shown in Fig. 4. In terms of blocking voltage, a higher CSL doping has two effects: It increases the electric field within the CSL region, but it also increases the critical electric field for avalanche breakdown. Since the first effect is more important than the second, the blocking voltage, which is limited by avalanche breakdown for a JFET width of $1\text{ }\mu\text{m}$, falls sharply with the CSL doping, as shown in Fig. 4. For these parameters, the optimum CSL doping is approximately $1 \times 10^{17}\text{ cm}^{-3}$.

A JFET width of $1\text{ }\mu\text{m}$ can protect the gate oxide up to JFET dopings of $1.5 \times 10^{17}\text{ cm}^{-3}$. Increasing the JFET doping beyond this point increases the oxide field drastically and, thereby, reduces the oxide-limited blocking voltage, as shown in Fig. 5. A JFET doping below $1.5 \times 10^{17}\text{ cm}^{-3}$ has little effect on the blocking voltage, since it is now determined by avalanche breakdown. Increasing the JFET doping reduces the JFET resistance and, thereby, reduces the total ON-resistance. For these parameters, the optimum JFET doping is approximately $1 \times 10^{17}\text{ cm}^{-3}$.

The new device with optimum doping concentrations for each epilayer and a JFET width of $1\text{ }\mu\text{m}$ is theoretically capable of blocking 1230 V with a specific ON-resistance of $6.88\text{ m}\Omega \cdot \text{cm}^2$. Since we are currently approaching the theoretical limit of 4H-SiC and each component of the ON-resistance has nearly attained its lowest value, it is difficult to reduce the ON-resistance further. At this point, cell pitch plays an important role since the specific ON-resistance of the device is directly proportional to the cell pitch. Past devices [5] have typically been fabricated with alignment tolerances of $2\text{ }\mu\text{m}$. With these rather loose tolerances, the cell pitch of the optimized device is $17\text{ }\mu\text{m}$. Two alignment tolerances in particular, the gate-source separation L_{GS} and the gate source overlap L_{GO} , consume $8\text{ }\mu\text{m}$, which is nearly half the total cell pitch. Modern optical lithography can easily operate with tolerances of $0.5\text{ }\mu\text{m}$, which would reduce the cell pitch to $11\text{ }\mu\text{m}$. This results in nearly 35% reduction in the specific ON-resistance.

The p^+ contact to the p-base is another feature that contributes to the size of the cell. In the interdigitated finger layout considered here, the p^+ contact typically runs down the entire length of each source finger (c.f. Fig. 1). The problem with a continuous p^+ contact is that any misalignment between the n^+ source metal and the p^+ base contact metal reduces the source contact length and increases the source contact resistance dramatically. For DMOSFETs, the p^+ contact grounds the p-base to prevent an open-base breakdown of the parasitic bipolar transistor in the blocking state and to remove stored charge from the drain-base capacitor during switching. To minimize the area penalty of the p^+ contacts and to eliminate the effect of misalignment on the source resistance, a segmented p^+ contact is proposed. In this approach, p^+ contacts are placed along only about 25% of the finger length. In the portion of the source fingers that do not contain p^+ contacts, the source contact width is greater, and the misalignment is no longer a factor. This reduces the overall source contact resistance without increasing the cell pitch. As will be shown, the design blocking voltage was achieved in the experimental devices, indicating that the

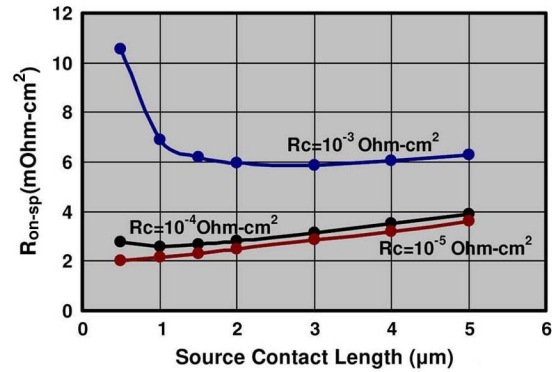


Fig. 6. Variation of $R_{ON,SP}$ with source contact length for different values of contact resistivity. In this comparison, L_P is $2\text{ }\mu\text{m}$, and L_{GS} , L_{GO} and L_{CH} are $0.5\text{ }\mu\text{m}$ each.

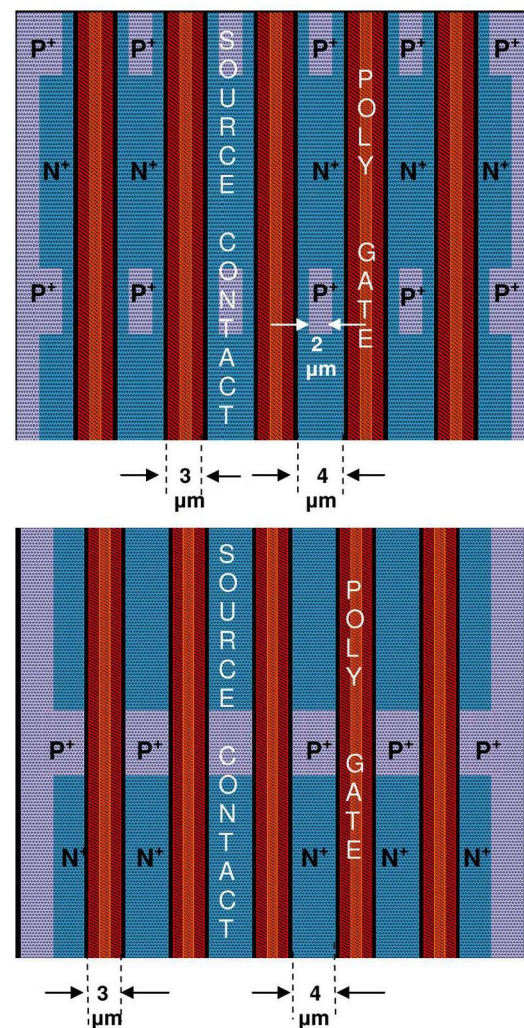


Fig. 7. (a) Layout of a device with small p^+ contacts (configuration "a"). (b) Layout of a device with large p^+ contacts (configuration "b").

parasitic bipolar effect is not exacerbated by the segmented contacts. The effect of the segmented p^+ contacts on switching performance was not investigated in this paper.

Source contact length L_S , as shown in Fig. 1, is another important parameter in the design. Longer source contact length reduces the total contact resistance, but increases the cell pitch. Optimum source contact lengths, which are determined for

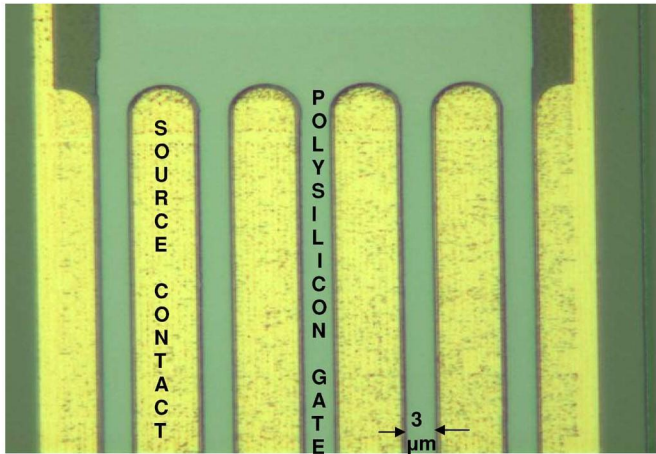


Fig. 8. Finished device with JFET width of $1\ \mu\text{m}$, gate length of $3\ \mu\text{m}$, gate–source separation of $0.5\ \mu\text{m}$, and a cell pitch of $10\ \mu\text{m}$.

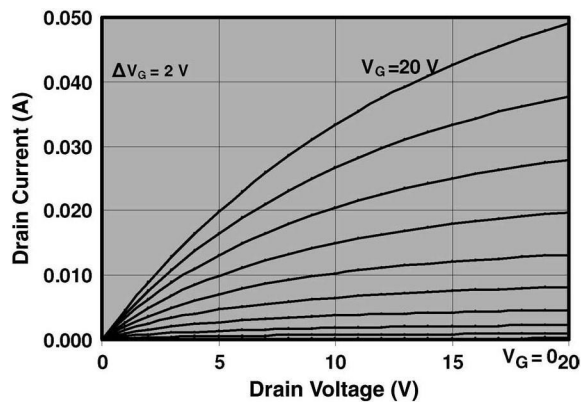


Fig. 9. ON-state characteristics of a device with JFET length of $1\ \mu\text{m}$ and active area of $0.32 \times 10^{-4}\ \text{cm}^2$. The specific ON-resistance is $6.95\ \text{m}\Omega \cdot \text{cm}^2$.

three values of contact resistivity, are shown in Fig. 6. It can be seen that reducing the source contact resistivity below about $1 \times 10^{-4}\ \Omega \cdot \text{cm}^2$ has little effect on the ON-resistance.

The final optimized device with segmented p^+ contacts and gate–source overlap and gate–source separation of $0.5\ \mu\text{m}$ has a device cell pitch of $8\ \mu\text{m}$, and the estimated specific ON-resistance is $3.89\ \text{m}\Omega \cdot \text{cm}^2$. The source contact length is $2\ \mu\text{m}$, with a contact resistivity of $5 \times 10^{-4}\ \Omega \cdot \text{cm}^2$.

III. DEVICE FABRICATION

The experimental devices are fabricated using a self-aligned technology [5] to produce a channel length at or below $0.5\ \mu\text{m}$. The starting wafer includes a $6\text{-}\mu\text{m}$ n-type epilayer that is doped at $1 \times 10^{16}\ \text{cm}^{-3}$ for the drift region and a $1\text{-}\mu\text{m}$ n-type epilayer that is doped at $1 \times 10^{17}\ \text{cm}^{-3}$ to form the CSL and JFET regions. The implant mask for the p-base is created by depositing $1.5\ \mu\text{m}$ of polysilicon. This polysilicon layer is patterned using a Ti/Ni mask defined by electron beam lithography. For comparison purposes, devices with JFET widths of 1 , 1.5 , and $2\ \mu\text{m}$ are fabricated. After p-base implantation, the Ti/Ni layer is removed, and the polysilicon layer is oxidized to expand its width by a controllable amount. A lateral growth of nearly $0.3\ \mu\text{m}$ is measured for devices with JFET width of $1\ \mu\text{m}$; for

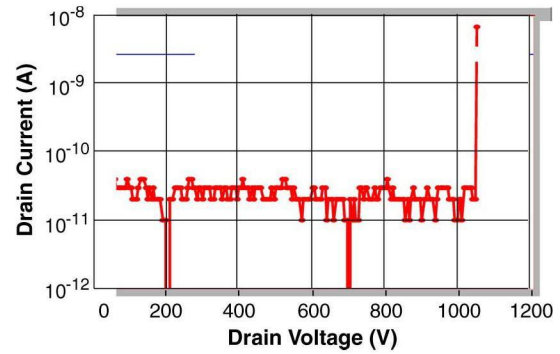


Fig. 10. Blocking characteristics of the device in Fig. 9.

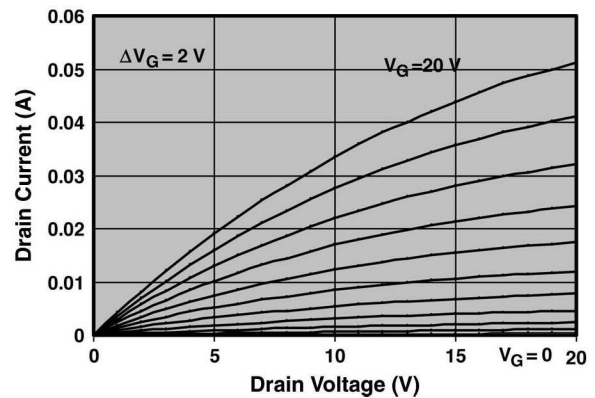


Fig. 11. ON-state characteristics of a device with JFET length of $1.5\ \mu\text{m}$ and active area of $0.34 \times 10^{-4}\ \text{cm}^2$. The specific ON-resistance is $8.1\ \text{m}\Omega \cdot \text{cm}^2$. This device has large p^+ contacts (configuration “b”).

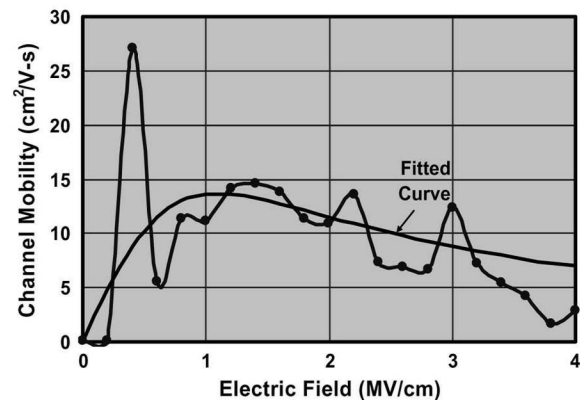


Fig. 12. Measured field-effect mobility as a function of gate electric field.

other devices with larger JFET widths, the expansion is nearly $0.4\ \mu\text{m}$. The oxidized polysilicon layer is then used as a mask for the n^+ source implantation. In this way, the lateral growth of the polysilicon layer defines the MOSFET channel length. A Ti/Au mask is used for the subsequent p^+ implantation. All the implants are annealed in an Ar ambient at $1600\ ^\circ\text{C}$ for 5 min.

A $1.5\text{-}\mu\text{m}$ deep trench is used for the edge termination and is created by reactive ion etching using a Ti/Ni mask. The wafer is subsequently oxidized in a pyrogenic system at $1150\ ^\circ\text{C}$ for two and half hours to form a 50-nm gate oxide, which is then NO annealed at $1175\ ^\circ\text{C}$ for 2 h. The final oxide thickness,

TABLE I
COMPARISON BETWEEN SIMULATED AND EXPERIMENTALLY MEASURED SPECIFIC ON-RESISTANCES

	Simulated				Experimental
Contact Resistivity [$\Omega\text{-cm}^2$]	5×10^{-4}	1×10^{-3}	5×10^{-4}	1×10^{-3}	1×10^{-3}
Channel mobility [$\text{cm}^2/\text{V}\cdot\text{s}$]	20	20	Measured	Measured	Measured
Specific On-resistance [$\text{m}\Omega\text{-cm}^2$]	3.89	5.38	4.53	6.02	6.95

which is calculated from C - V measurements, is 52 nm. To achieve a gate-source overlap and a gate-source separation of 0.5 μm , the gate, p^+ , and source contacts are defined using electron beam lithography. Phosphorous-doped polysilicon is used as the gate electrode. Two different configurations of p^+ contacts are used, as shown in Fig. 7(a) and (b). P^+ implants as well as p^+ contacts for devices with configuration “a” are defined by electron beam lithography to minimize misalignment between the source and p^+ contacts. Each p^+ contact in the configuration shown in Fig. 7(a) is 2- μm wide and 4- μm long, and the contacts are inserted at intervals of 20 μm . The second configuration shown in Fig. 7(b) has a contact width that is the same as the source contacts, and a length along the finger direction of 6 μm . The contacts are inserted at 30- μm intervals along the finger. Devices with configuration “b” are expected to have slightly higher ON-resistance than those of configuration “a”, since the source current contribution is negligible from the part of the device finger where the p^+ contacts are located. A Ti (15 nm)/Al (75 nm)/Ni(50 nm) metal stack is used for the p^+ contact, whereas 100 nm of Ni is used as the n^+ contact. All contacts are annealed in vacuum at 950 $^\circ\text{C}$ for 2 min, and a Ti (15 nm)/Au (400 nm) stack is used as the top metal. Fig. 8 shows a finished device with a gate length (L_G in Fig. 1) of 3 μm and a gate source separation of 0.5 μm . The channel length for all devices is approximately 0.3 μm .

IV. DEVICE CHARACTERIZATION

DMOSFETs with JFET widths of 1 μm and type “a” p^+ contacts show a specific ON-resistance of 6.95 $\text{m}\Omega\cdot\text{cm}^2$ for a blocking voltage of 1050 V, as shown in Figs. 9 and 10. The blocking voltage is limited by the avalanche breakdown, with a gate oxide field of less than 4 MV/cm. DMOSFETs with JFET widths of 1.5 and 2 μm show specific ON-resistances of 7.5 and 7.9 $\text{m}\Omega\cdot\text{cm}^2$, respectively. The current in these devices is nearly independent of the JFET width; therefore, it is the cell pitch that makes the difference in the specific ON-resistance.

The lowest values of specific ON-resistance obtained for the devices with type “b” p^+ contacts are 8.1 and 8.3 $\text{m}\Omega\cdot\text{cm}^2$ for JFET widths of 1.5 and 1 μm , respectively. ON-state characteristics of a device with JFET width of 1.5 μm are shown in Fig. 11.

Since we did not consider the edge termination of the devices in our simulations, the actual blocking voltage is expected to be 70%–80% of the simulated result of 1230 V. The fabricated devices exhibit slightly higher ON-resistance than predicted by

the simulations. This is attributed to a slightly high n^+ contact resistivity and slightly lower inversion channel mobility. An n^+ contact resistivity of $5 \times 10^{-4} \Omega\cdot\text{cm}^2$ is assumed for the simulation, whereas the contact resistivity that is estimated from transmission-line method testers on the experimental wafer is $1 \times 10^{-3} \Omega\cdot\text{cm}^2$. An effective inversion layer electron mobility of 20 $\text{cm}^2/\text{V}\cdot\text{s}$ is assumed for the simulations, independent of oxide field. The inversion channel mobility is experimentally measured on lateral MOSFETs with channel lengths of 70, 90, 110, and 130 μm using a constant current technique [4]. These test MOSFETs are fabricated in ion-implanted p-wells and are adjacent to the experimental DMOSFETs. The peak value of the measured inversion channel mobility is found to be 15 $\text{cm}^2/\text{V}\cdot\text{s}$, as shown in Fig. 12. To reconcile the simulations with measurements, the optimized device is further simulated using the fitted curve in Fig. 12 to represent the inversion layer mobility and with contact resistivity of $1 \times 10^{-3} \Omega\cdot\text{cm}^2$ for n^+ and p^+ contacts. Table I shows a comparison of the simulated and experimental results. This comparison indicates that relatively high contact resistivity and low inversion channel mobility contributed an additional 1.5 and 0.7 $\text{m}\Omega\cdot\text{cm}^2$, respectively, to the total specific ON-resistance. The remaining difference between the simulated and measured specific ON-resistances may be due to a slightly narrower JFET width in the experimental devices due to lateral straggle of the p-well implant.

V. CONCLUSIONS

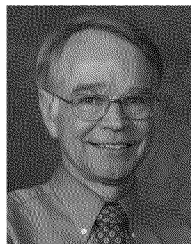
A detailed simulation study is conducted to optimize the ON-state performance of 4H-SiC short-channel DMOSFETs for a blocking voltage of 1 kV. The optimized device is fabricated and exhibits a specific ON-resistance of 6.95 $\text{m}\Omega\cdot\text{cm}^2$ and an avalanche breakdown voltage of 1050 V, with a gate oxide field of less than 4 MV/cm at breakdown. The optimized device has a figure of merit $V_B^2/R_{\text{ON,SP}}$ of 159 MW/cm^2 , which is nearly a factor of two higher than our previously reported short-channel 4H-SiC DMOSFET on a 6- μm epilayer.

ACKNOWLEDGMENT

The authors would like to thank J. Hughes for his valuable technical assistance and advice, Prof. M. A. Capano for the implant annealing, and J.-Y. Lee for the assistance with ohmic contact annealing. The electron beam lithography was performed in the Microelectronics and Nanotechnology Laboratory at the University of Illinois at Urbana-Champaign.

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